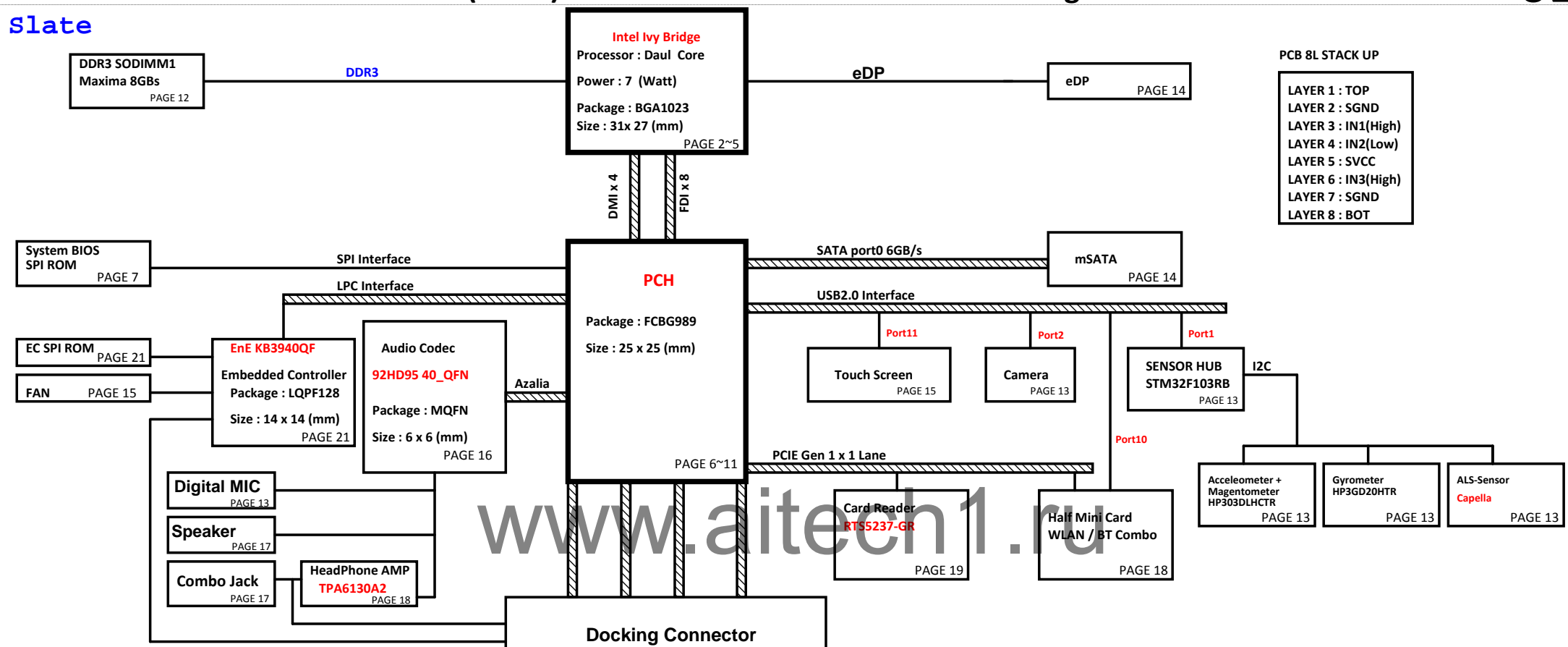


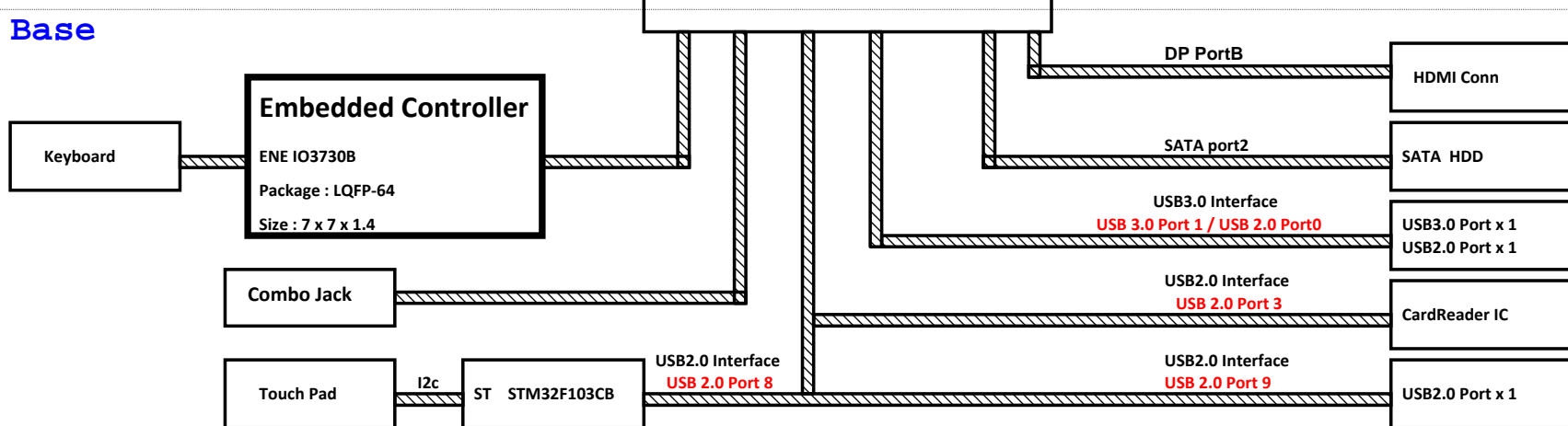
Wolverine (13.3") Intel Chief River Platform Block Diagram

01

Slate



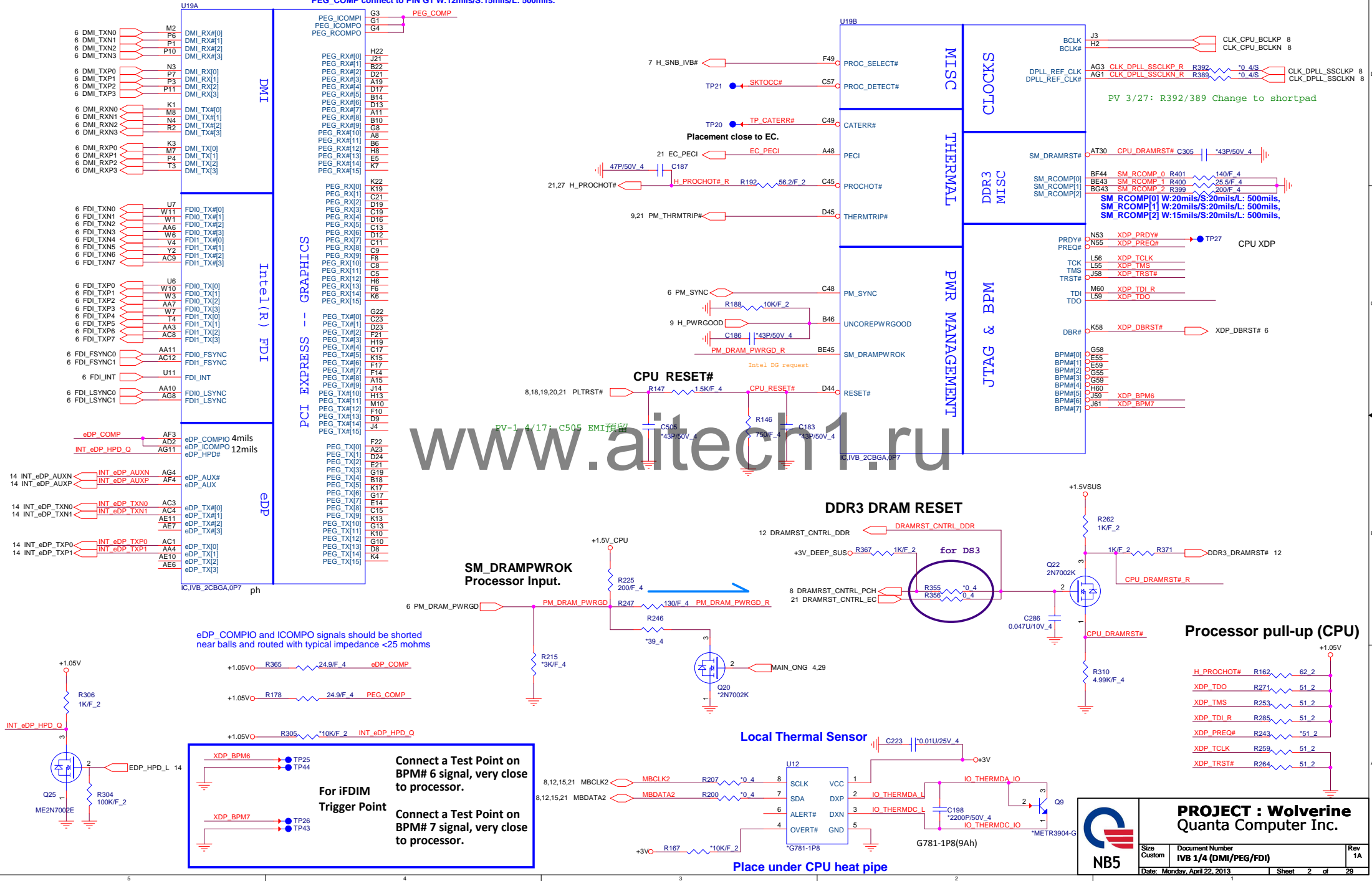
Base



Ivy Bridge Processor (DMI,PEG,FDI)

02

PEG_COMP connect to PIN G3/G4 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN G1 W:12mils/S:15mils/L: 500mils.

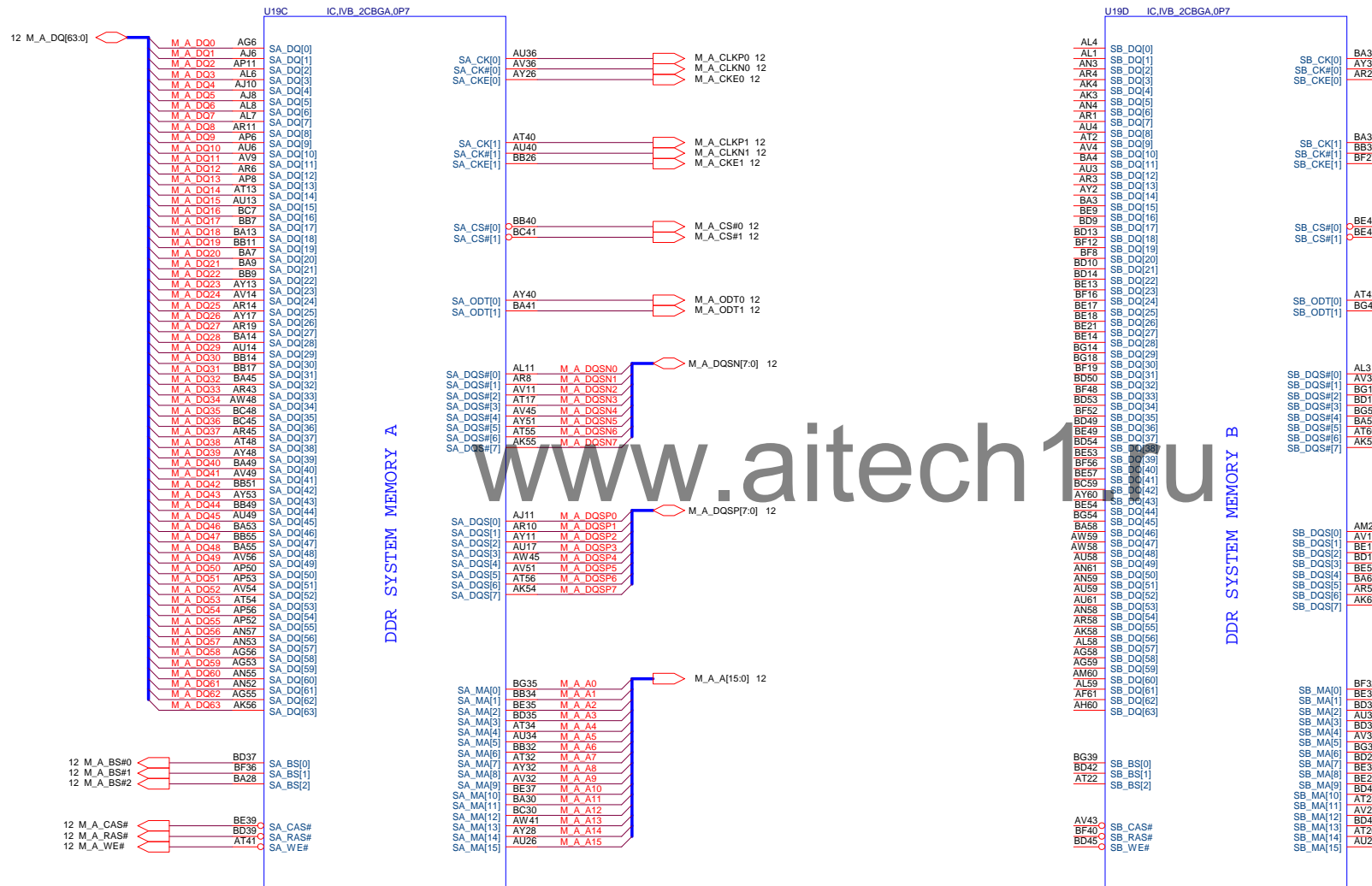


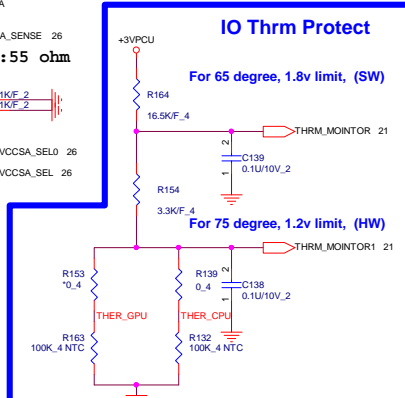
www.aitech1.ru

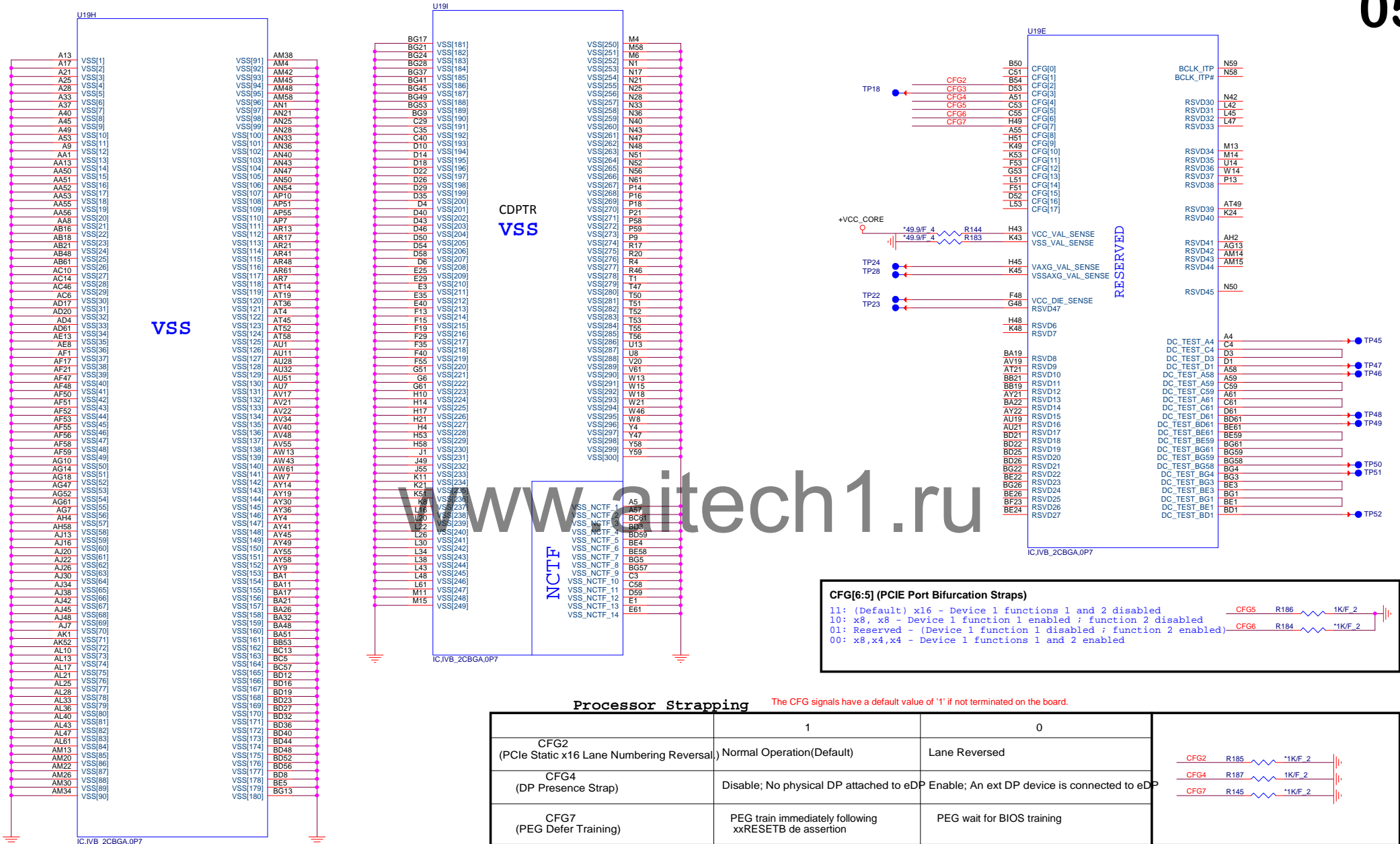
PROJECT : Wolverine
Quanta Computer Inc.

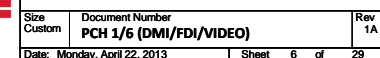
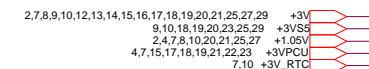
Size Custom	Document Number IVB 1/4 (DMI/PEG/FDI)	Rev 1A
Date: Monday, April 22, 2013	Sheet 2 of 29	

Ivy Bridge Processor (DDR3)



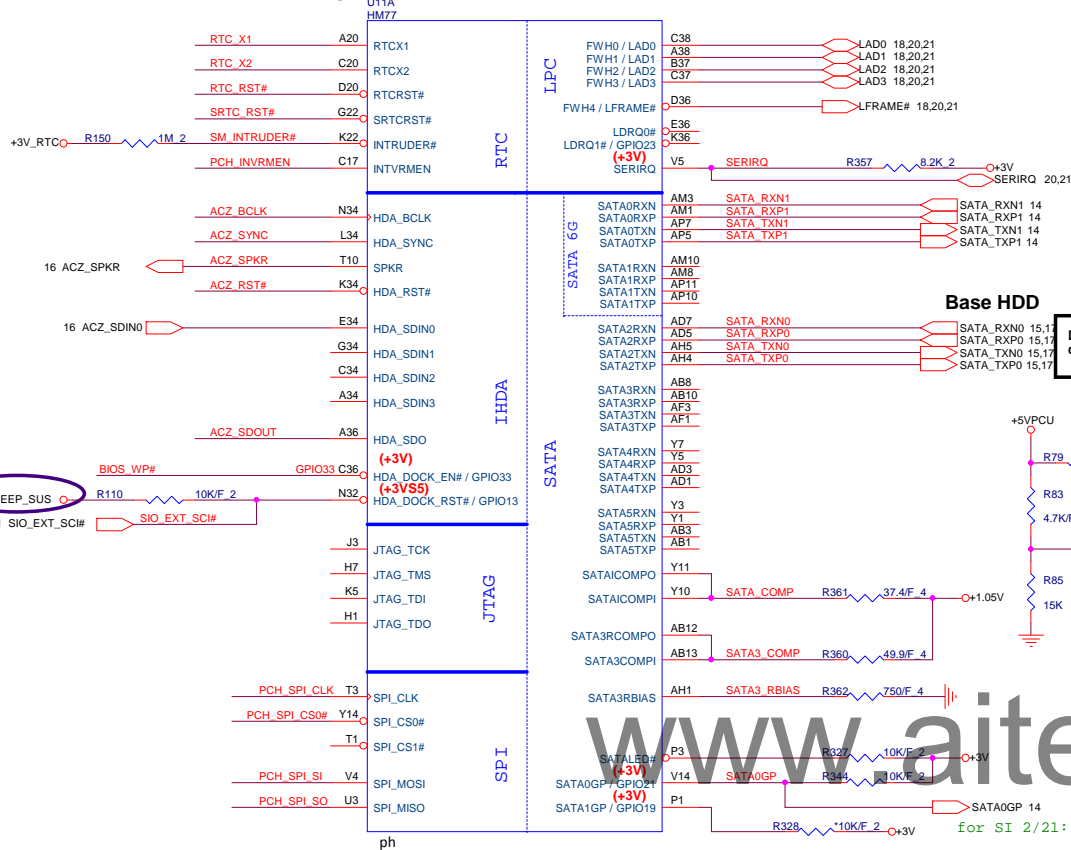






Cougar Point/Panther Point (HDA,JTAG,SATA)

07



mSATA (SATA 6Gb/s)

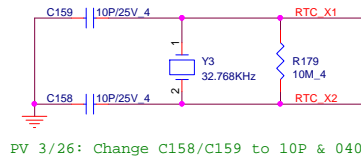
Base HDD

DG recommended that SATA AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

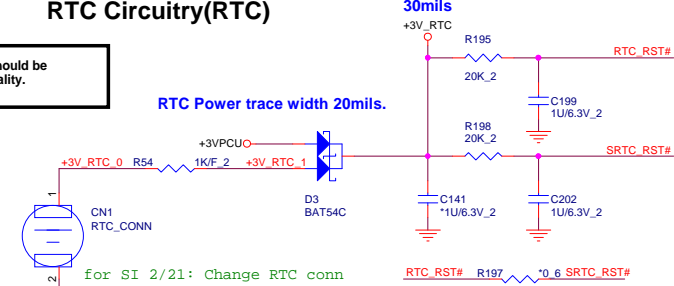
RTC Power trace width 20mils.

for SI 2/21: add SATA0GP

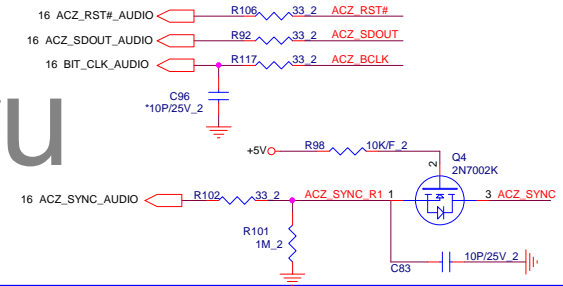
RTC Clock 32.768KHz



RTC Circuitry(RTC)



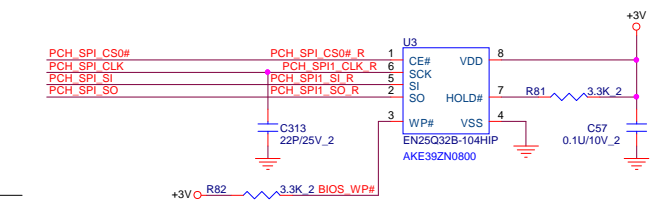
HDA Bus(CLG)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R249 1K/F 2 ACZ_SPKR									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V R40 10K/F 2 PCL_GNT3# 8									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R201 330K 4 PCH_INVRMEN									
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R90 1K/F 2 ACZ_SDOUT GPIO33_EC 21									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr><tr><td>1</td><td>0</td><td>SPI</td></tr><tr><td>0</td><td>1</td><td>LPC</td></tr></table>	GNT1#	GNT0#	Boot Location	1	0	SPI	0	1	LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GNT1#	GNT0#	Boot Location											
1	0	SPI											
0	1	LPC											
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+3V R323 2.2K 2 R324 1K/F 2 NV_CLE 9 H_SNB_IVB# 2									
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	for DS3 +3V_DEEP_SUS R84 1K/F 2 ACZ_SYNC									
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V_DEEP_SUS R81 1K/F 2 ACZ_SDOUT									
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										

Vender	Size	P/N	PCH SPI ROM(CLG)
EON	4MB	AKE39ZN0Q02 (EN25Q32B-104HIP)	
MX	4MB	AKE39FP0Z02 (MX25L3206EM2I-12G)	
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)	
Socket		DFHS08FS023(91960-0084L-8P-SOCKET)	



PROJECT : Wolverine
Quanta Computer Inc.

Size Custom

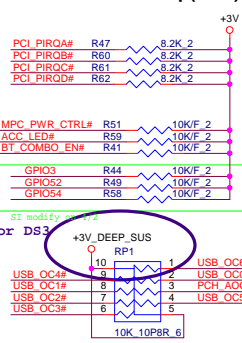
Document Number
PCH 2/6 (SATA/HDA/SPI)

Date: Monday, April 22, 2013

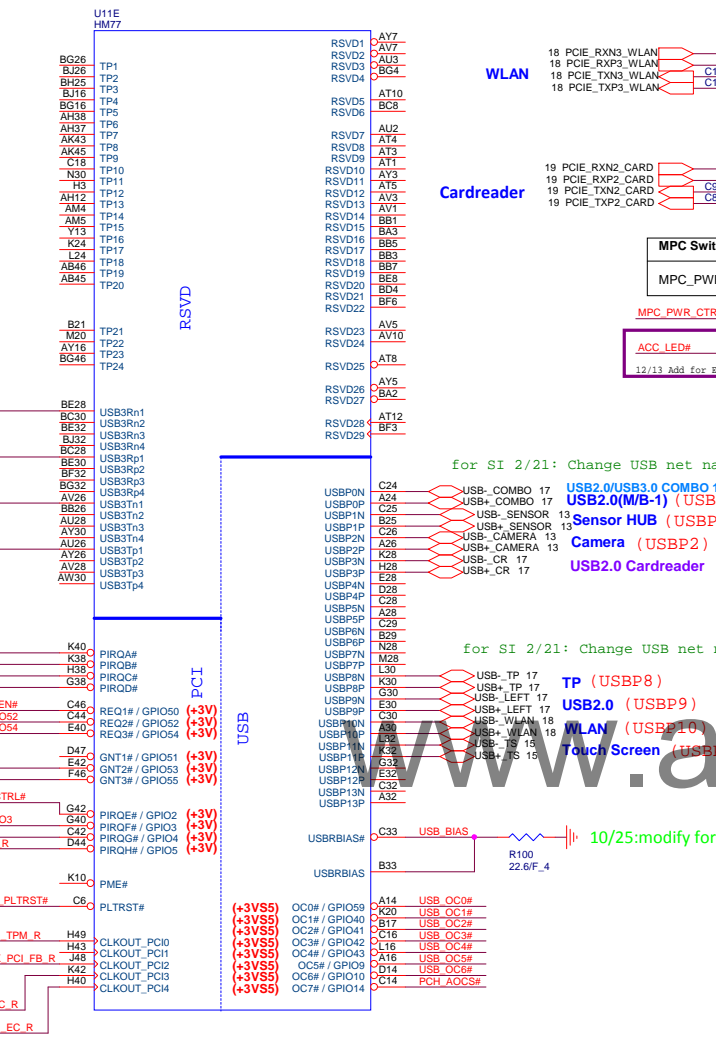
Rev 1A

Sheet 7 of 29

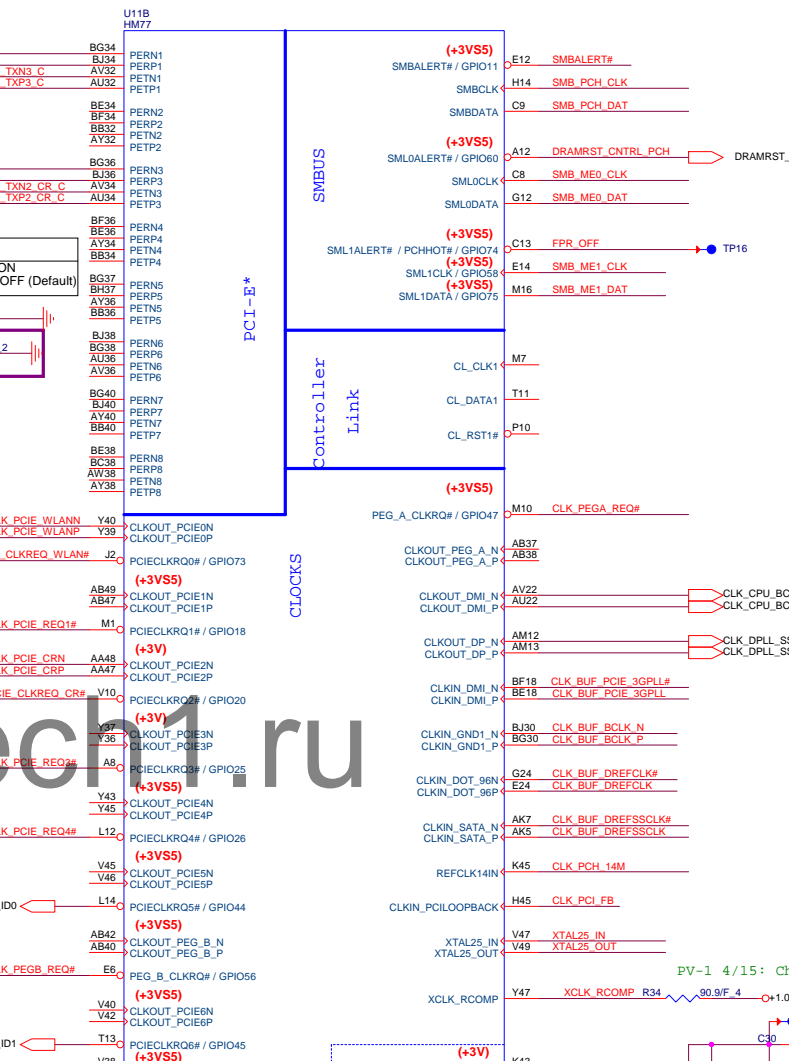
PCI/USB OC# Pull-up (CLG)



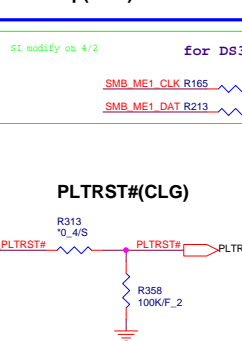
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



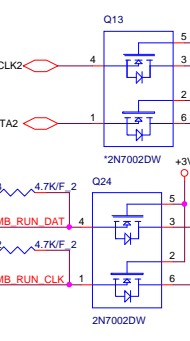
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



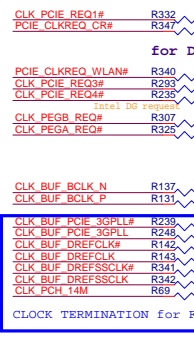
Push/Pull-up(CLG)



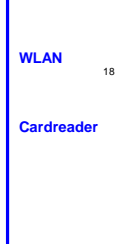
SMBus/Pull-up(CLG)



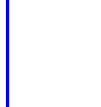
CLK_REQ/Strap Pin()



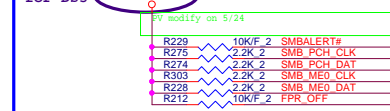
PCIE Clock



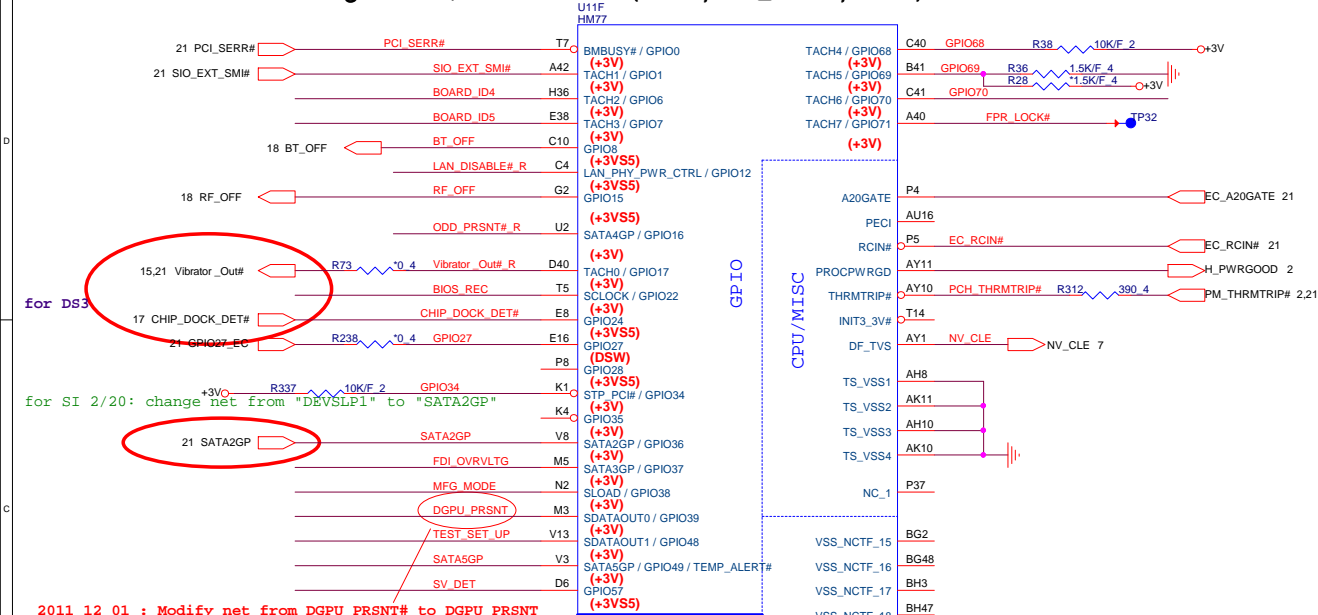
Cardreader



for DS3 **+3V_DEEP_SUS** **SMBus/Pull-up(CLG)**



Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

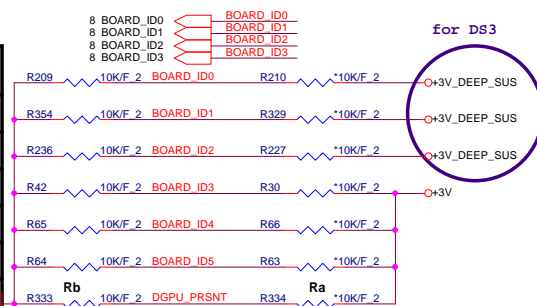


OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

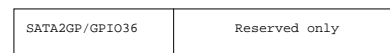
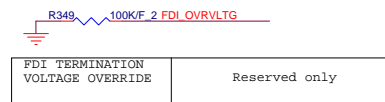
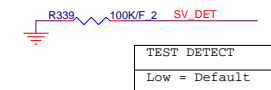
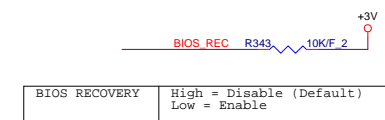
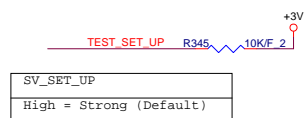
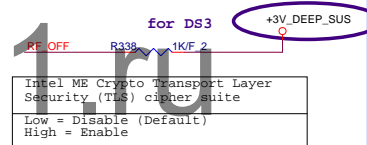
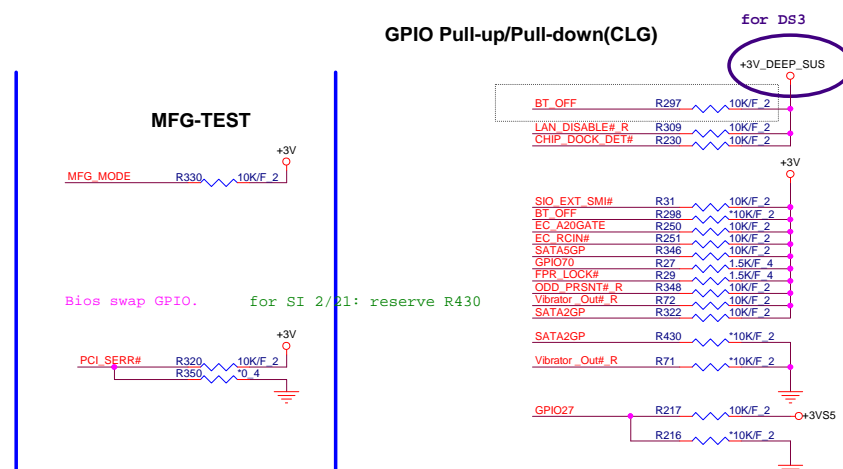
Chief River BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4 14": 0 15": 1	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0 UMA: 0 DIS: 1
U62 UMA	0	0	0	0	0	0
U62 DIS	0	0	0	0	0	1
14"	0	0	0	0	0	0
15.6"	0	1	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0

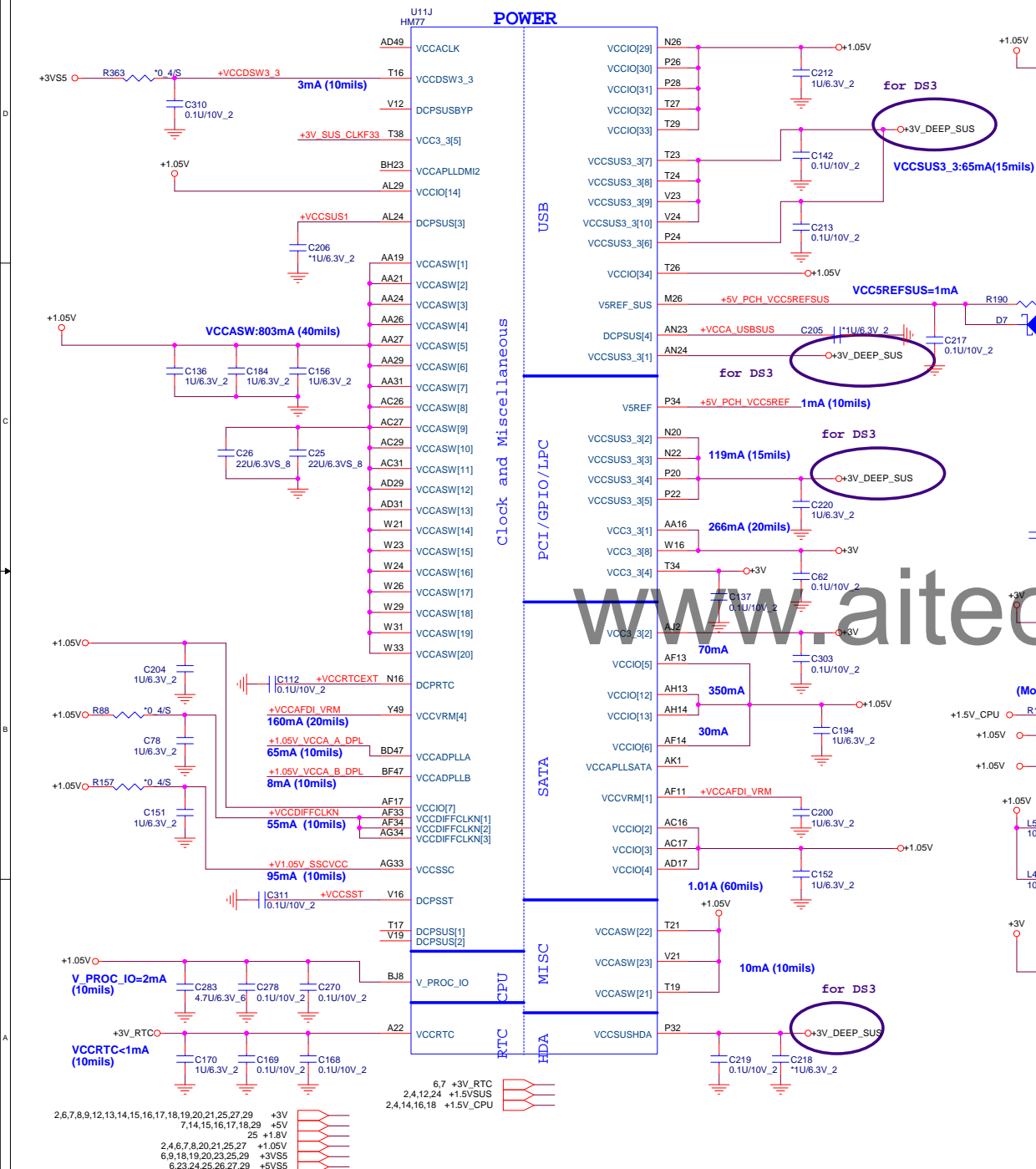
	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra



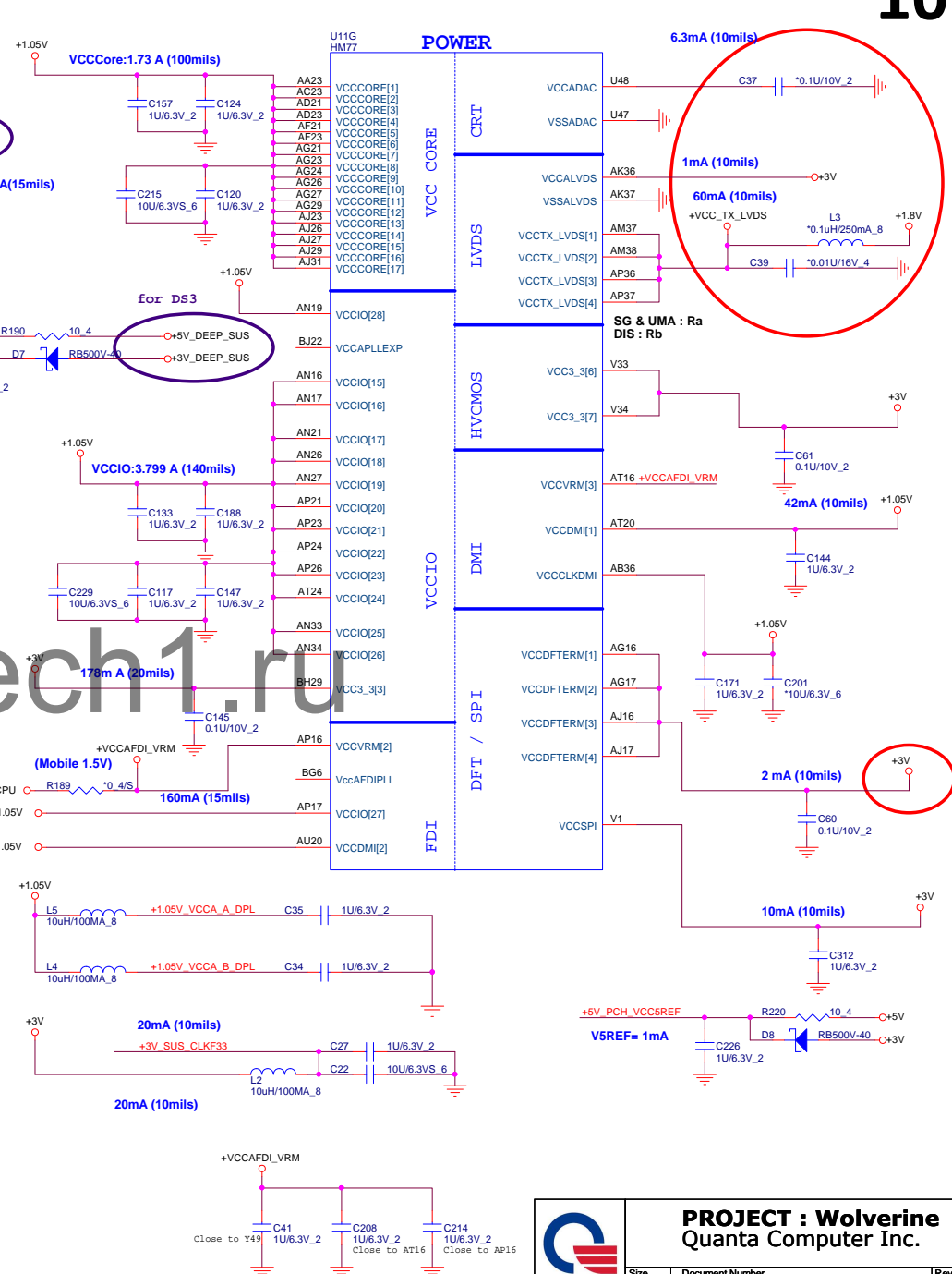
GPIO Pull-up/Pull-down(CLG)



Cougar Point/Panther Point (POWER)

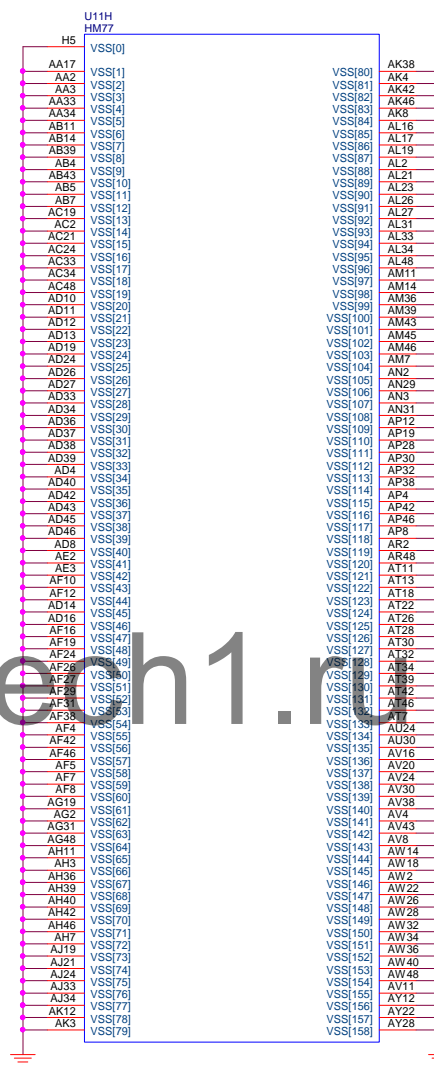
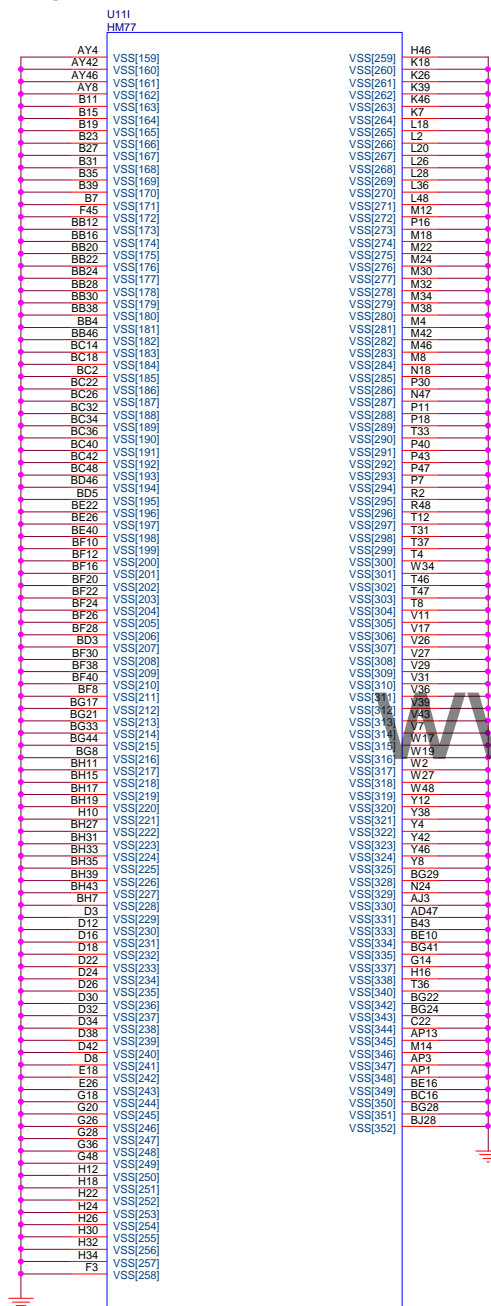


Cougar Point/Panther Point (POWER)



Cougar Point/Panther Point (GND)

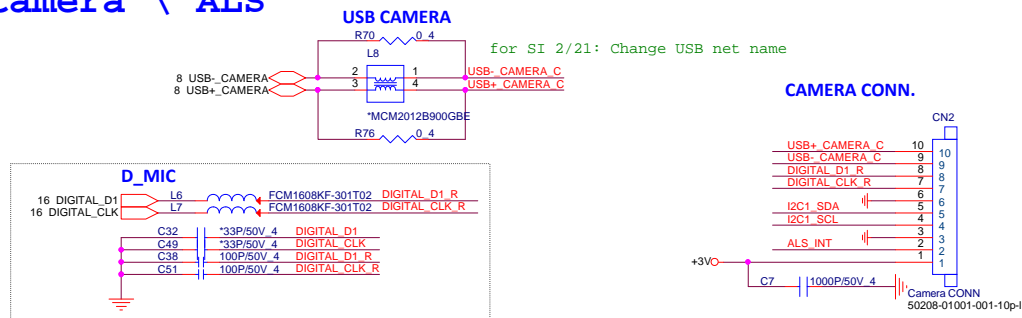
Cougar Point/Panther Point (GND)



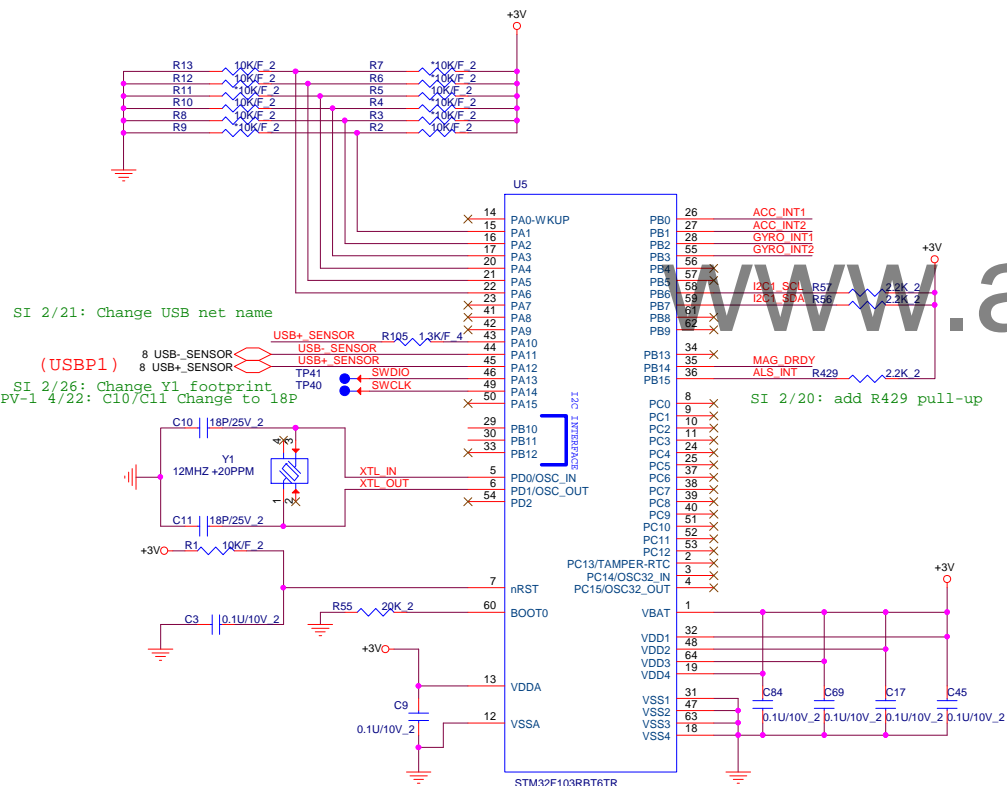


Size Custom	Document Number DDR3 DIMMO-STD(4.0H)	Rev 1A
Date: Monday, April 22, 2013	Sheet 12 of 29	

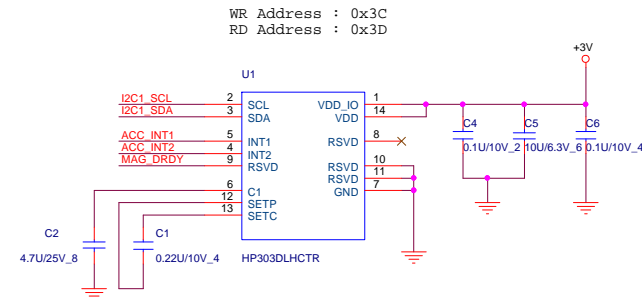
Camera \ ALS



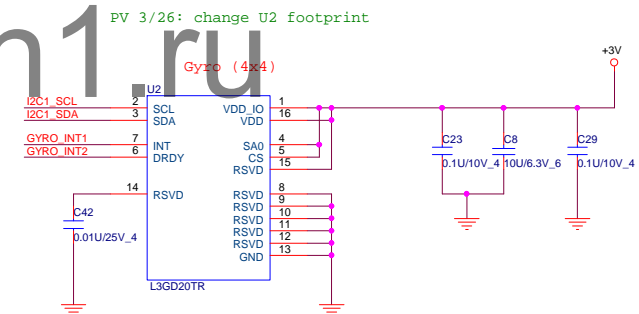
Sensor HUB

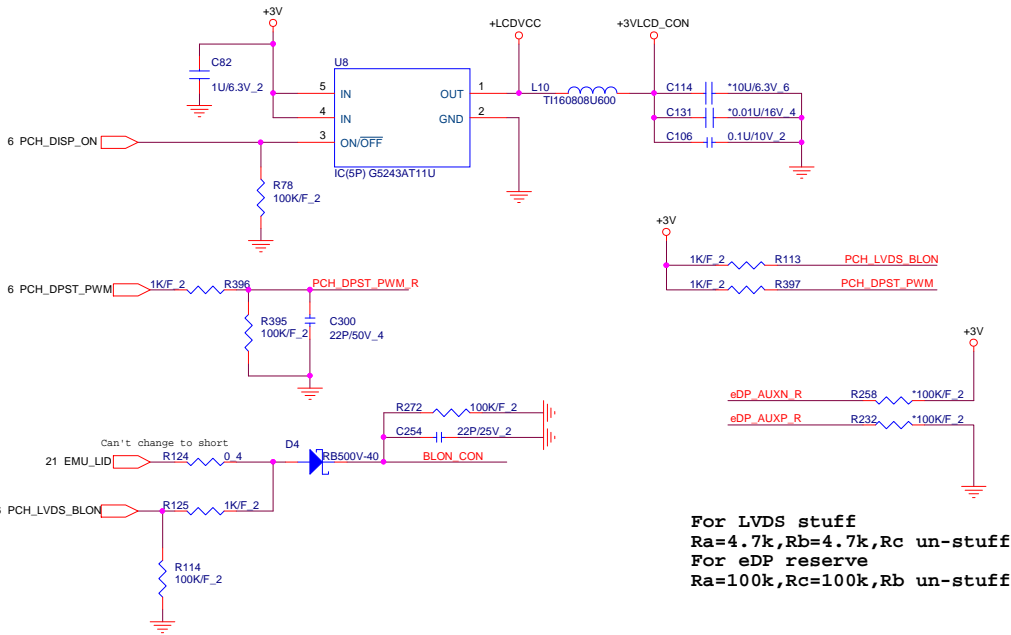


G-sensor / E-compass



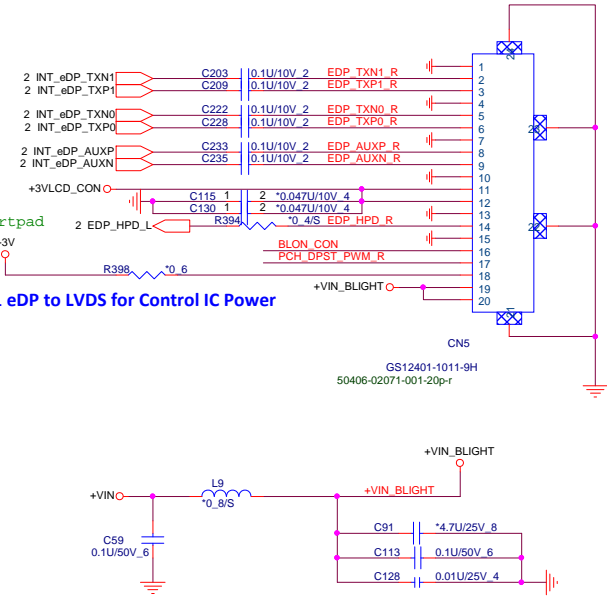
Gyro





PV 3/27: R394 Change to shortpad

DV1 eDP to LVDS for Control IC Power

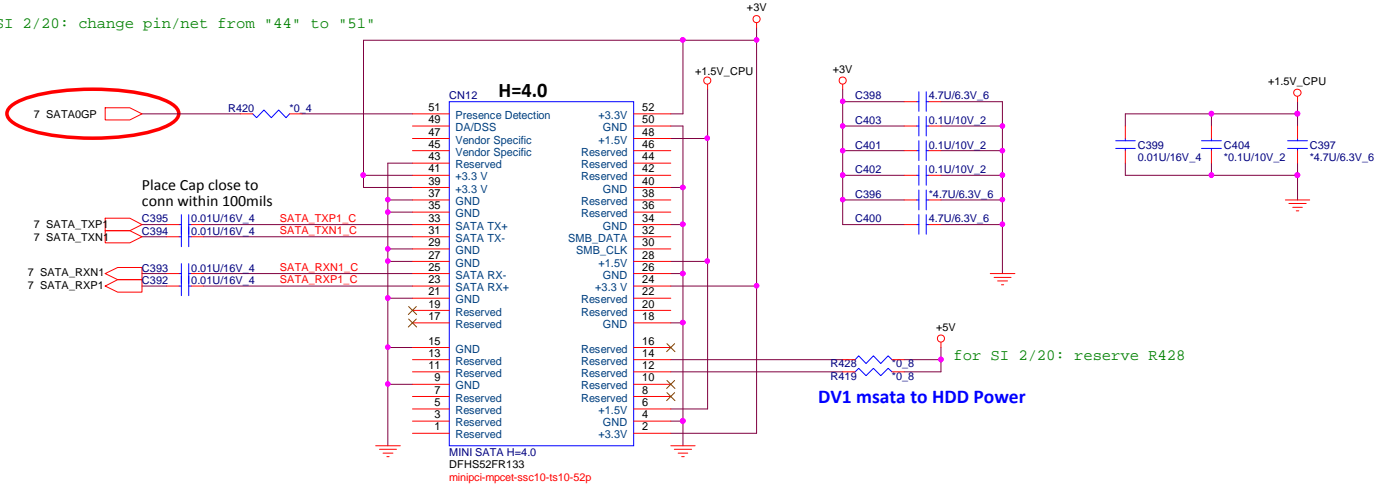


For LVDS stuff
Ra=4.7k,Rb=4.7k,Rc un-stuff
For eDP reserve
Ra=100k,Rc=100k,Rb un-stuff


Mini PCI-E Card 2- Full size mSATA

www.aitech1.ru

for SI 2/20: change pin/net from "44" to "51"



2,6,7,8,9,10,12,13,15,16,17,18,19,20,21,25,27,29	+3V
4,7,15,17,18,19,21,22,23	+3VPCU
7,10,15,16,17,18,29	+5V
20,22,23,24,25,27,28,29	+VIN
6,23,24,25,26,27,29	+5VSS

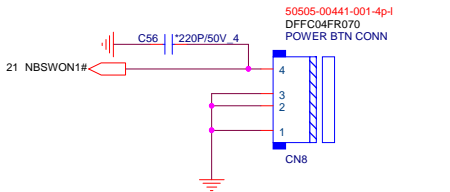


PROJECT : Wolverine
Quanta Computer Inc.

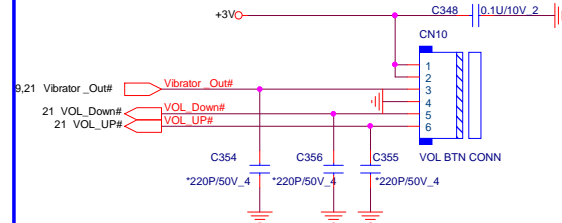
Size Custom	Document Number eDP / mSATA	Rev 1A
Date: Monday, April 22, 2013		Sheet 14 of 29

Control Buttons

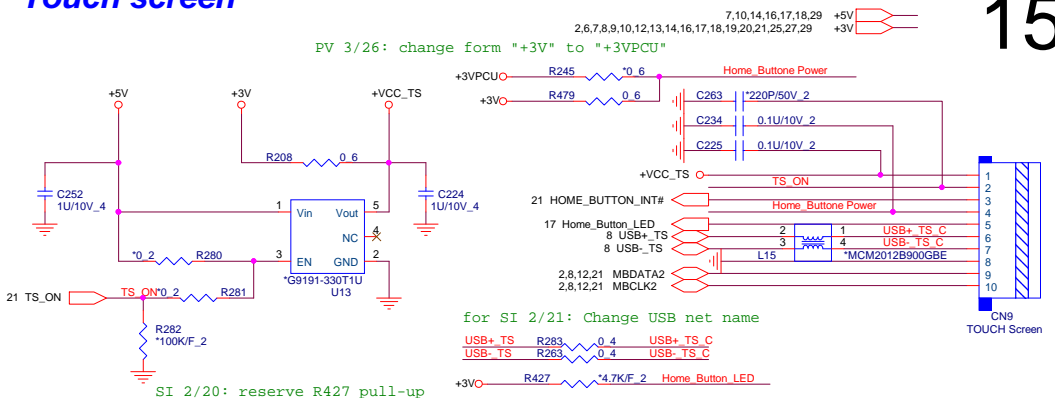
Power button



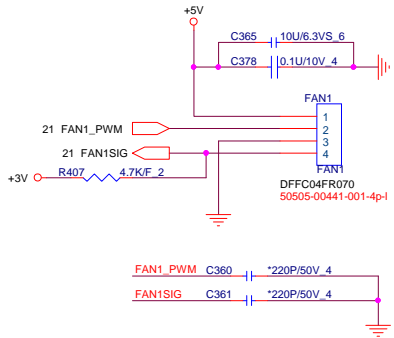
VOL BTN CONN



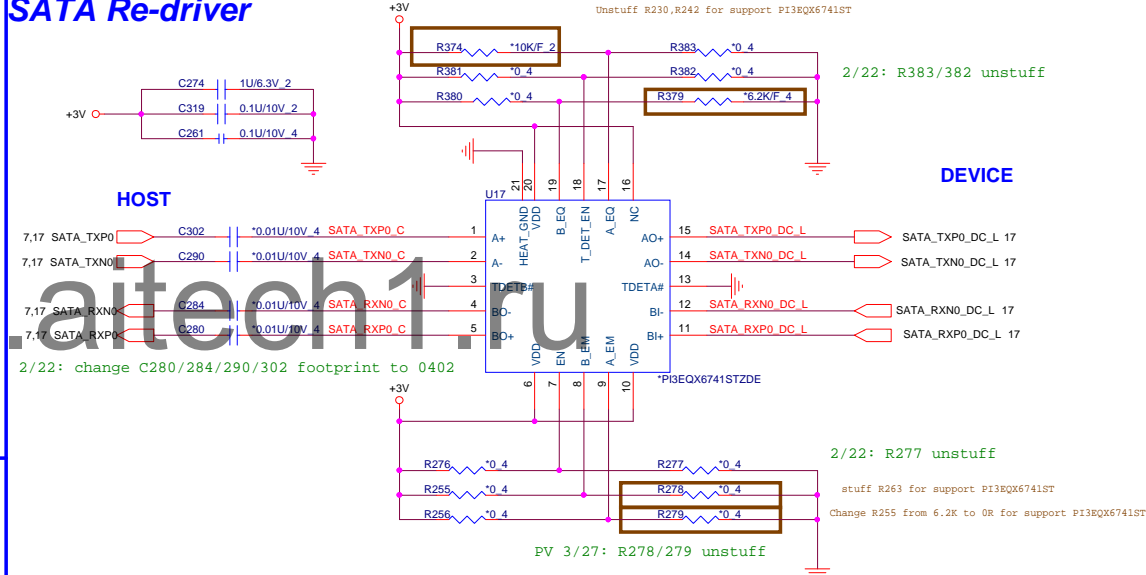
Touch screen

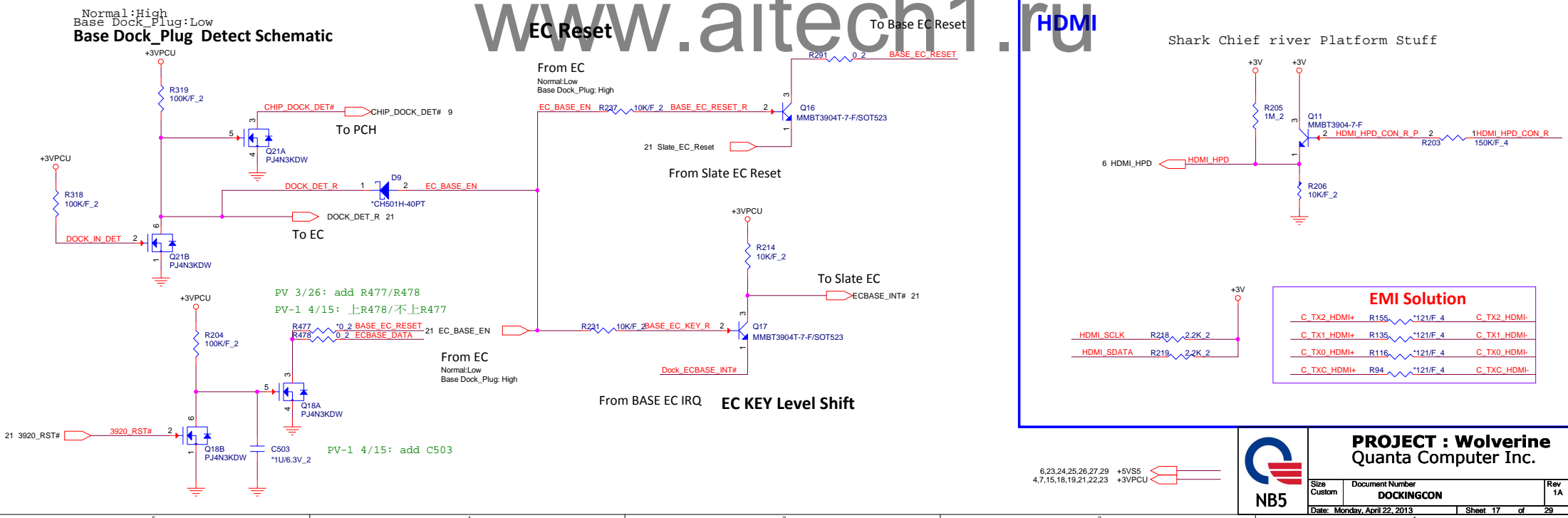
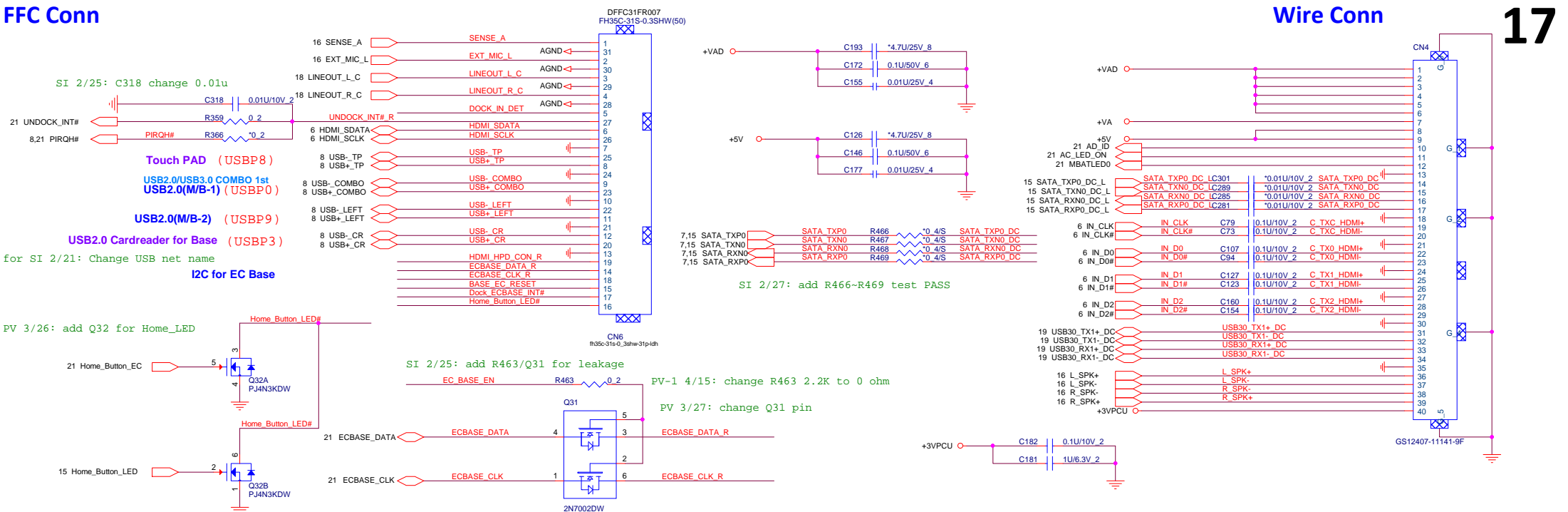


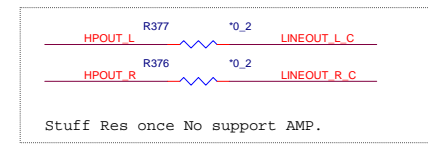
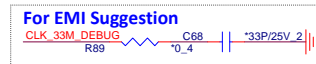
FAN



SATA Re-driver

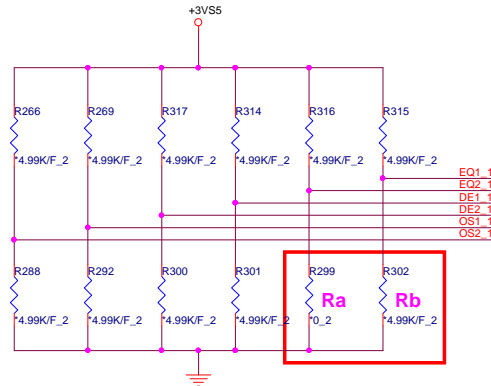




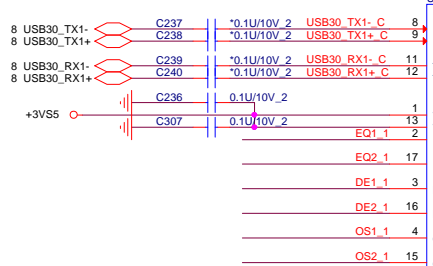


USB 3.0 Re-driver

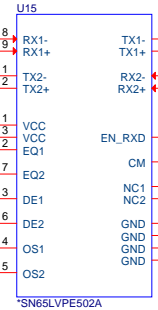
OSx		Transition Bit Amplitude	
NC(default)		1000	
0		870	
1		1085	
EQx		Equalization dB	
NC(default)		0	
0		7	
1		15	
DEx	OSx=NC	OSx=0	OSx=1
NC	-3.5dB	-2.2dB	-4.4dB
0	-6.0dB	-5.2dB	-6.0dB
1	-8.5dB	-8.9dB	-7.6dB
EN_RXD		DEVICE FUNCTION	
1(default)		Normal operating mode	
0		Sleep mode	
CM		DEVICE FUNCTION	
0(default)		Normal operating mode	
1		Compliance mode	



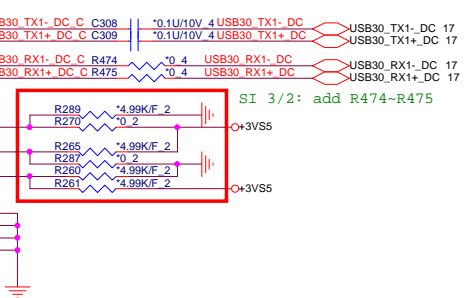
HOST



USB3.0 re-driver IC



DEVICE



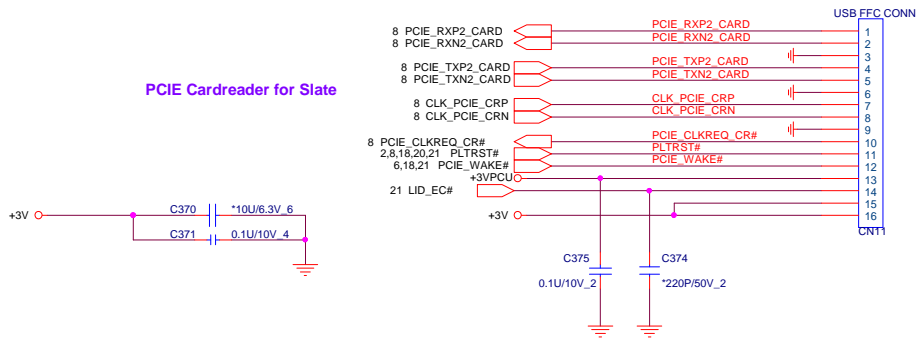
USB30_TX1- R470 *0.4/S USB30_TX1- DC
 USB30_TX1+ R471 *0.4/S USB30_TX1+ DC
 USB30_RX1- R472 *0.4/S USB30_RX1- DC
 USB30_RX1+ R473 *0.4/S USB30_RX1+ DC

SI 3/1: add R470~R473 test PASS

CardReader

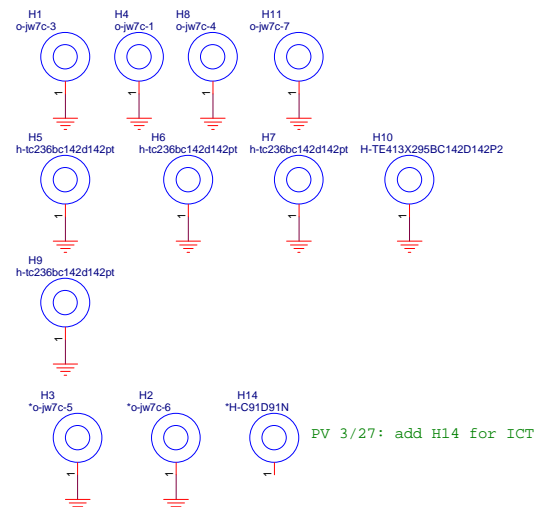
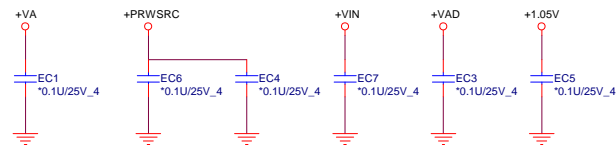
www.aitech1.ru

PCIE Cardreader for Slate



6,9,10,18,20,23,25,29 +3V55

EMI / Hole



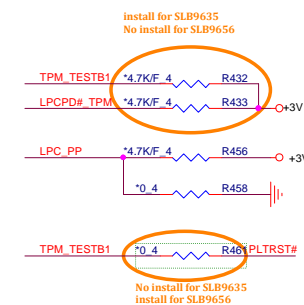
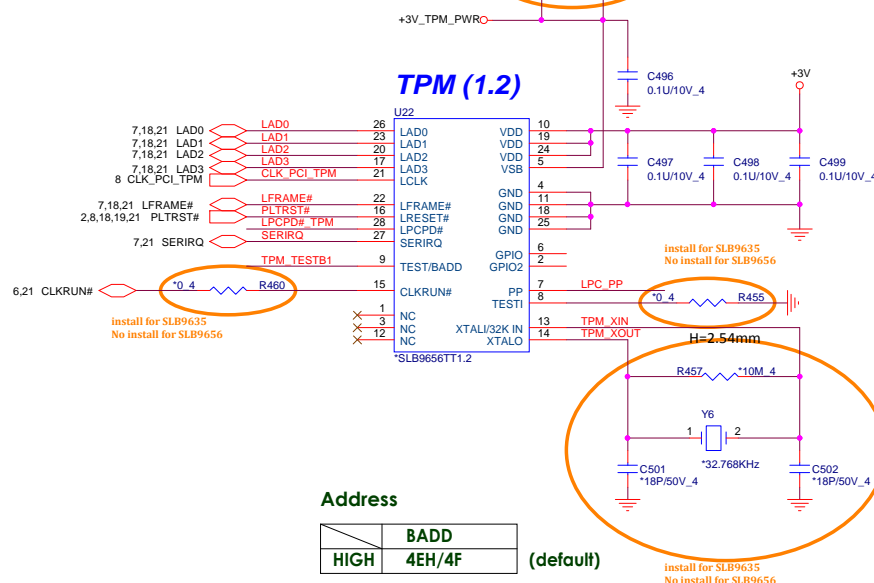
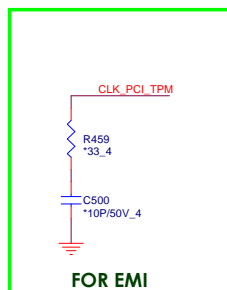
TPM

SI 2/25: add TPM function

+3V rail for SLB9656

+3VS5 rail for SLB9635

www.aitech1.ru

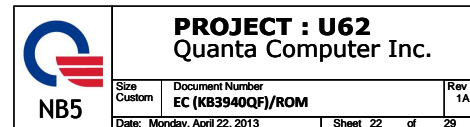


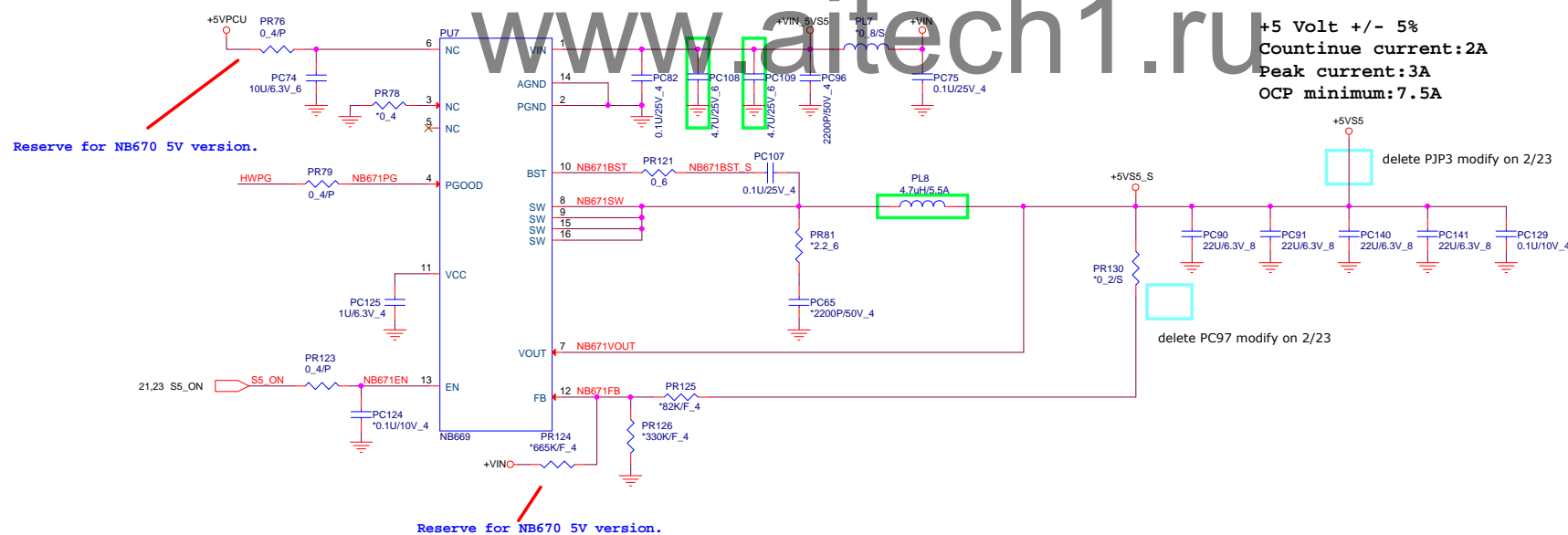
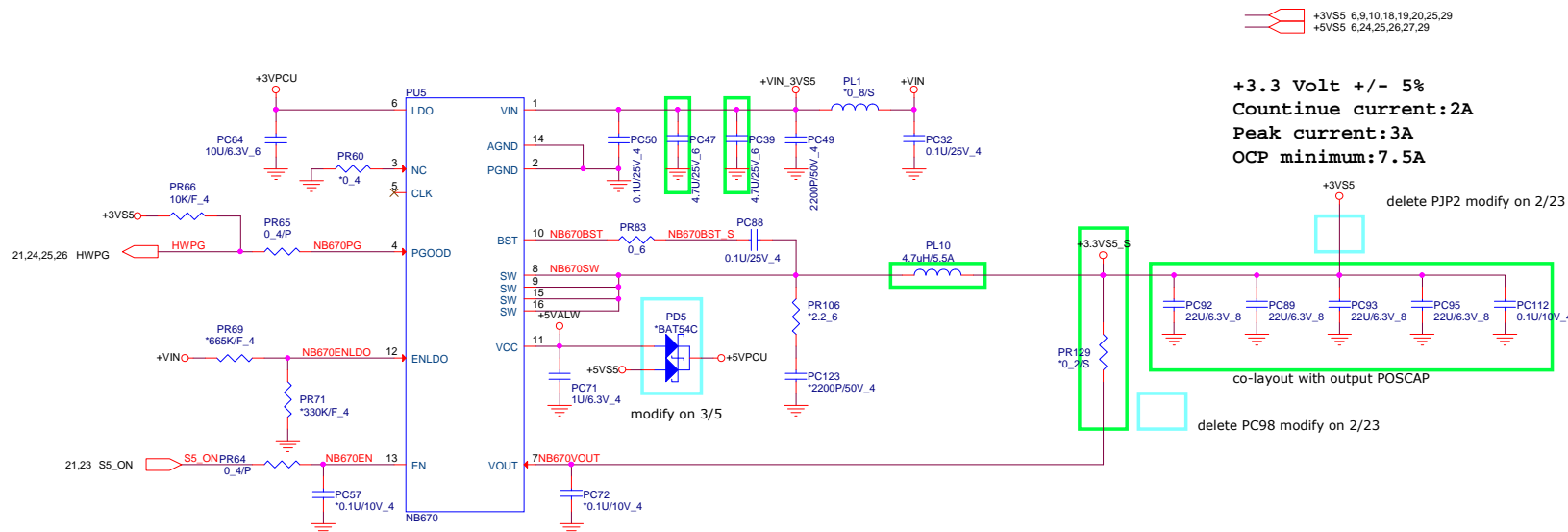
	SLB9635	SLB9656
R458	Install	No install
R453	No install	Install
R454	Install	No install
R455	Install	No install
Y6, R413	Install	No install
C501, C502	Install	No install
R412	Install	No install
R409	Install	No install
R457	No install	Install

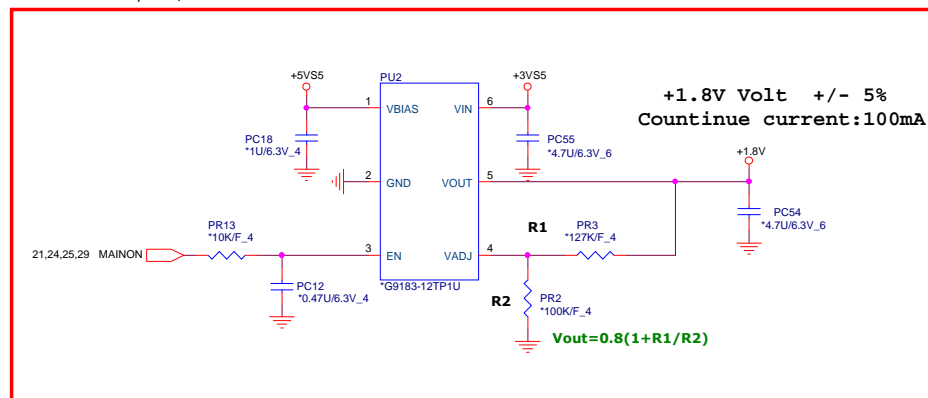
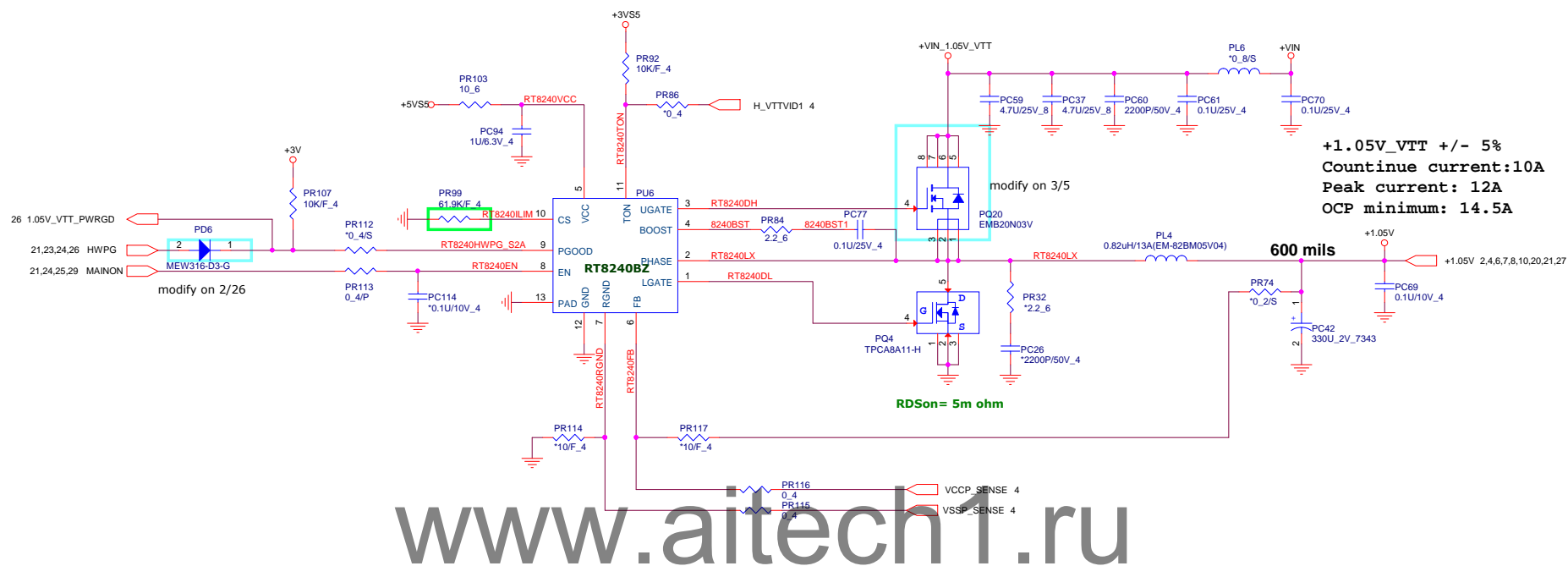
Address

	BADD
HIGH	4EH/4F

(default)



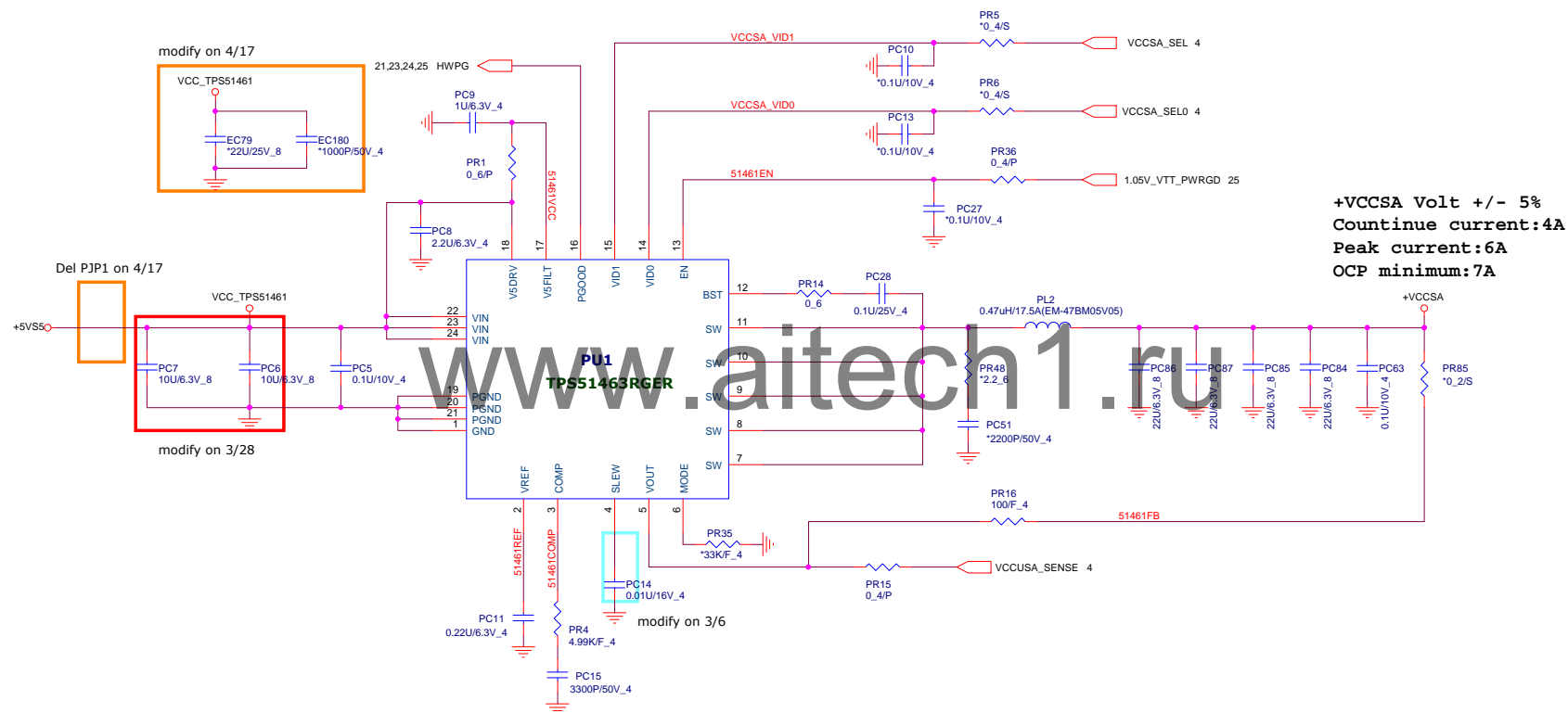


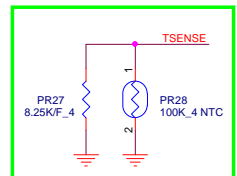
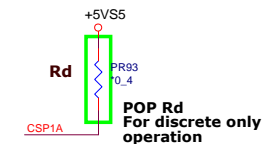
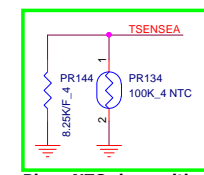
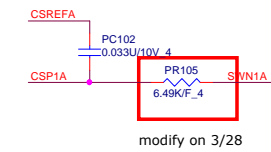
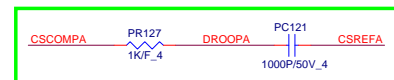
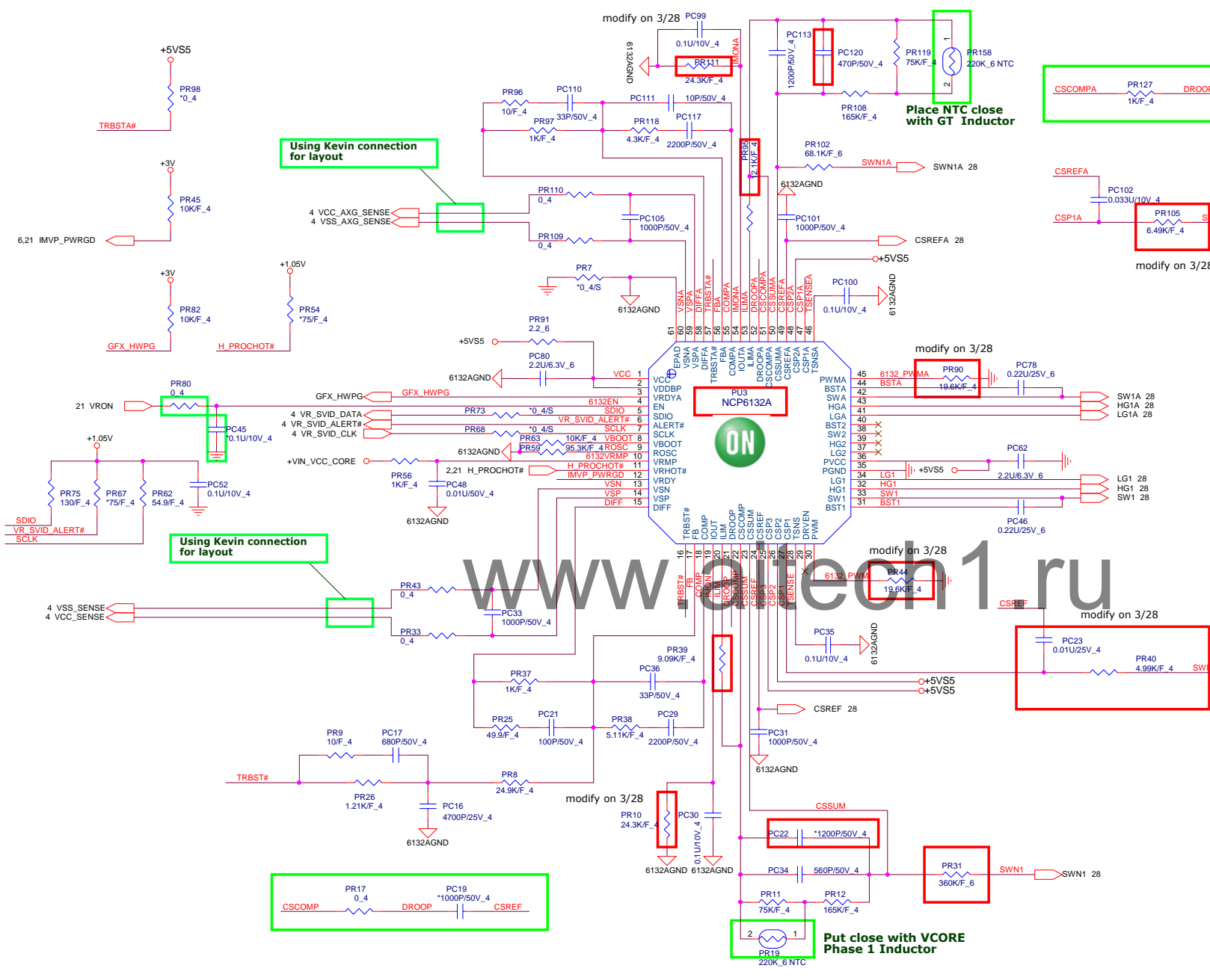



TPS51463RGER/AL051463000

For CPU ULV system agent
voltage slew rate of 0.5 -10 mV/ μ s

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V





			PROJECT : U62 Quanta Computer Inc.	
Size	Document Number	Rev		
Custom	CPU Core1 (NCP6132B)	1A		
Date: Monday, April 22, 2013	Sheet	27 of 29		

